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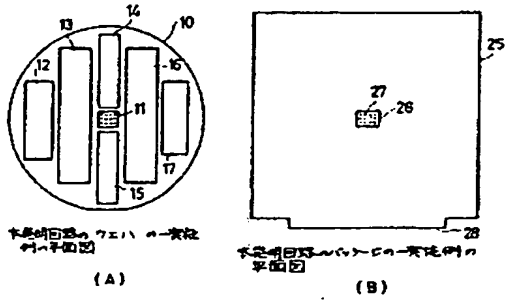
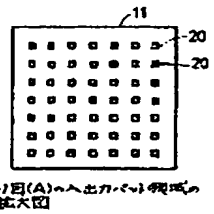
TITLE : WAFER-SCALE SEMICONDUCTOR INTEGRATE CIRCUIT





ABSTRACT : PURPOSE: To realize a wafer-scale circuit as well as to improve the yield of bumps by a method wherein a wafer is placed on a package to connect the bumps of input/output pads with pads to correspond to the input/output pads.

CONSTITUTION: An input/output pad region 11 is formed at the central position of a circuit forming part of a wafer 10 excepting the vicinity of the peripheral edge part of the wafer and circuit blocks 12–17 are formed on the periphery of the region 11. Input/output pads 20 are provided uniformly at equal intervals within the region and solder bumps are each formed on the pads 20. A package lead region 26 is provided at the central position of a package 25, the region 26 is positioned corresponding to the region 11 of the wafer 10 and the region 26 is provided with pads 27 of a plurality of package leads, which correspond to the pads 20 in a ratio of 1 to 1. The wafer 10 is placed on the package 25 making the pads 20 of the region 11 correspond to the pads 27 of the region 26 and the solder bumps of the pads 20 are heat-bonded to the pads 27. A water- scale circuit can be realized in such a way and at the same time, the yield of the bumps can be improved.